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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/859,484	05/18/2001	Hideo Shibahara	01FN008US	4513

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EXAMINER	
QI, ZHI QIANG	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 04/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/859,484	Applicant(s) SHIBAHARA ET AL.	
	Examiner Mike Qi	Art Unit 2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *2,3,5,6,8,9,11 and 12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,7,10 and 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 24, 2004 has been entered.

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4, 7, 10 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant admitted prior art (AAPA) in view of US 6,429,918 (Choi et al), US 6,281,953 (Lee et al) and US 6,335,772 (Sato et al).

Claim 1, AAPA discloses (page 1, line 13 – page 8, line 8; Figs.3-5) a conventional IPS mode liquid crystal display structure comprising:

- a first transparent substrate (1) including: a plurality of gate lines (6) and a plurality of drain lines (5) formed on the substrate (1); thin film transistors (TFT 4) being connected to the gate lines (6) and the drain lines (5); pixel electrodes (3) being formed within the pixel region enclosed with an adjacent pair of the gate lines (6) and an adjacent pair of the drain lines (5), and connected to the TFT (4); and common electrodes (2) developing an electric field within each of the pixel regions between the pixel electrode and itself;
- a second transparent substrate (14) opposing to the first substrate (1) including: color layers (12) provided for each of the pixel regions;
- a black matrix layer (13) overlapping the gate lines (6) and the drain lines (5);
- liquid crystal (10) provided in a space between the first substrate (1) and the second substrate (14).

AAPA does not expressly disclose that the color layer being spaced apart from the gate lines and the drain lines when seen on a plane, i.e., the color layers do not overlap the gate lines and the drain lines; and the black matrix layer and the drain lines (or gate lines) constituting direct capacitive coupling free from any electrode therebetween.

However, Choi discloses (col.3, line 60 – col.5, line 64; Figs.2-3) that the color filters (34) are formed at both sides of a sub-pixel defined by the black matrix (33), and the color filters (34) do not overlap the data line (13). According to the Fig.2, the gate lines (11) are extended in the x direction and the data lines (13) are extended in y

direction, thereby defining sub-pixels, such that the color filters (34) do not overlap the gate lines (11) and the data lines (13).

Choi indicates (col.5, lines 25-64) that such structure would reduce the light leakage, and the parasitic electric field generating region is shield by the black matrix (33), and there is no influence at leakage current. Therefore, such structure would reduce the parasitic electric field, and improving the aperture ratio.

A lacking limitation is such that the capacitive coupling free from any electrode between the black matrix and the signal line, and as seen in Fig.3 of Choi, a shielding electrode (37) is between black matrix (33) and drain line (13).

However, Lee discloses (col.3, line 49 – col.6, line 21: Fig.3D) that a structure of a liquid crystal display device in which the black matrix layer (41) and the gate line (22) (same as the drain line 27) constituting direct capacitive coupling free from any electrode therebetween, and such liquid crystal display structure having high aperture ratio and high transmittance.

Still lacking limitation is such that the resistance value of the black matrix is between 10^2 and 10^5 Ω cm.

However, Sato discloses (col.3, line 58 – col.4, line 18) that the electrically-conductive light-shielding layer preferably has a sheet resistance not higher than (less than or equal to) 100 Ω/□ , so that the resistance value of 100 Ω/□ for the light shielding layer is an overlap or lie inside range as the resistance value of 10^2 Ω cm, and in the case where the claimed range "overlap or lie inside range discloses by the prior art" a prima facie case of obviousness exists (see MPEP 2144.05. I).

Sato indicates (col.3, line 58 – col.4, line 18) that such electrically-conductive light-shielding layer restricts the coupling capacitance with the adjacent wiring.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to arrange the color layers do not overlap the gate lines and data lines and having resistance value as claimed in claim 1 for reducing the parasitic electric field and achieving high aperture ratio and high transmittance, and restricting the coupling capacitance with the adjacent wiring.

Claim 4, AAPA discloses (paragraph 0064) that according to the reference JP 5-249436, the driving method for the liquid crystal display is using a driving circuit to apply voltage to each pixel while inverting the polarities of the applied voltage between the odd-numbered gate lines and even-numbered gate lines, i.e., per scanning cycle, and that is a dot inversion driving method, and the same driving is carried frame by frame, so that the applied voltage is averaged for all the display pixels, thereby suppressing the flickers.

Claims 7 and 10, AAPA discloses (paragraph 0004) that the IPS mode liquid crystal display having comb-teeth-wise shape pixel electrode (3) and common electrode (2) in each pixel.

Claim 13, lacking limitation is such that the resistance value of black matrix is between 10^2 and 10^4 Ω cm.

However, Sato discloses (col.3, line 58 – col.4, line 18) that the electrically-conductive light-shielding layer preferably has a sheet resistance not higher than (less than or equal to) 100 Ω/□ , so that the resistance value of 100 Ω/□ for the light shielding

layer is an overlap or lie inside range as the resistance value of 10^2 Ω cm, and in the case where the claimed range "overlap or lie inside range discloses by the prior art" a prima facie case of obviousness exists (see MPEP 2144.05. I).

Response to Arguments

4. Applicant's arguments filed on March.24, 2004 have been fully considered but they are not persuasive.

Applicant's **only** arguments are as follows:

1) The references do not teach or suggest a resistance value of the black matrix is between 10^2 and 10^5 Ω cm.

Examiner's responses to Applicant's **only** arguments are as follows:

1) The reference Sato discloses (col.3, line 58 – col.4, line 18) that the electrically-conductive light-shielding layer preferably has a sheet resistance not higher than (less than or equal to) 100 Ω/□ , so that the resistance value of 100 Ω/□ for the light shielding layer is an overlap or lie inside range as the resistance value of 10^2 Ω cm, and in the case where the claimed range "overlap or lie inside range discloses by the prior art" a prima facie case of obviousness exists (see MPEP 2144.05. I). The reference Sato indicates (col.3, line 58 – col.4, line 18) that such electrically-conductive light-shielding layer restricts the coupling capacitance with the adjacent wiring.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Qi whose telephone number is (571) 272-2299. The examiner can normally be reached on M-T 8:00 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mike Qi
April 8, 2004

DUNG T. NGUYEN
PRIMARY EXAMINER